Design of "Universal Module" Based Time and Frequency System using White Rabbit Technology

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***Abstract*—In the WR network, a dedicated time and frequency system is set up to deliver and distribute the time signal from WR switches or WR nodes locally. Accordingly, the design of a flexible, transferrable, and extensible time and frequency system is required for complementing existing WR equipment and WR networks. Here we propose the concept of "universal module". Based on the universal modules, a variety of devices and TF system can be developed. In particular, three applications are demonstrated in this paper. Finally, the first measurement results of the integrated devices will be demonstrated in this paper.**

Keywords—White Rabbit; time and frequency transfer; frequency distribution; frequency stability measurement

I. INTRODUCTION

In recent years, White Rabbit (WR) is an emerging technique for accurate and precise time and frequency transfer over distributed network.

In the WR network, a dedicated time and frequency (TF) system is set up to deliver and distribute the time signal from WR switches or WR nodes locally, as well as monitor network performance. However, the existing commercial equipment could not fully satisfy the new demands on WR system due to their limitations in noise floor, integration, expenses, etc. Therefore, the design of a flexible, transferrable, and extensible time and frequency system is required for complementing existing WR equipment and WR networks.

II. THE CONCEPT OF "UNIVERSAL MODULE"

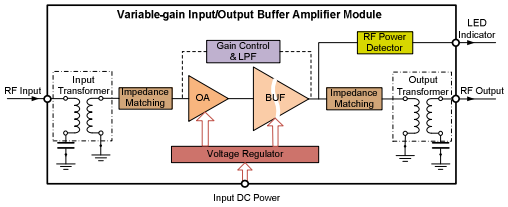
Here we propose the concept of "universal module". It can be defined as a functional platform which can work independently to perform specific functions, and its hardware and software are designed to allow flexible parameter updates and function extension.

Four functional modules are described in this section which includes: an input/output buffer module, an integral/fractional PLL module, a control and logic module, and a power regulator module.

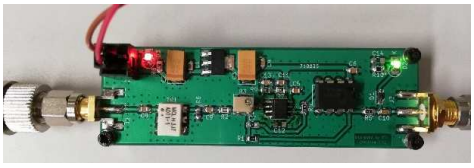
A. Input/Output buffer module

The input/output buffer module is a universal channel isolation buffer amplifier which isolates the back-stage circuit from the front-stage circuit. It also provides variable-gain and bandwidth limitation functions.

The structure and the prototype of the buffer amplifier module are shown in Figure 1. It consists of a RF transformer, an operational amplifier (OA) with gain control and a low pass filter (LPF), a high-speed buffer (BUF), and supported circuits such as impedance matching, RF power indicator and DC voltage regulator circuits. According to different applications, the bandwidth and gain can be tuned based on the same PCB. By this flexible design, the buffer module can be fit for widely used applications.



(a). Functional block diagram of input/output buffer module



(b). Prototype of input/output buffer module

Fig. 1: Input/Output buffer module

B. Integral/Fractional PLL module

The phase locked loop (PLL) module is a universal module which can be used as a low-noise integral or fractional frequency synthesizer. The low-noise PLL is widely used in the time and frequency devices for the purpose of frequency multiplication, precise signal tracking, phase and frequency offset tuning as well as clock signal generation.

The functional block diagram and the prototype of the PLL module are shown in Figure 2. This design allows flexible and wide range frequency and phase offset settings, as well as multiple data communication options. The PLL module mainly consists of two parts: the PLL circuit and the MCU control circuit. The PLL circuit is composed of a low-noise frequency synthesizer where both the output frequency and phase can be

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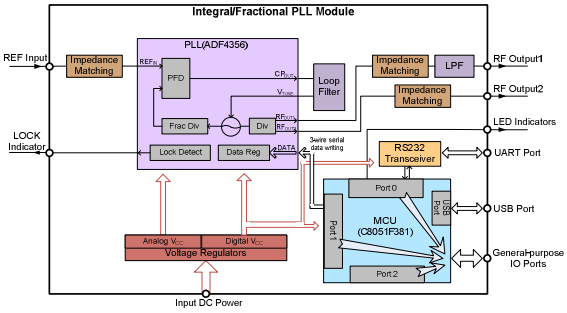
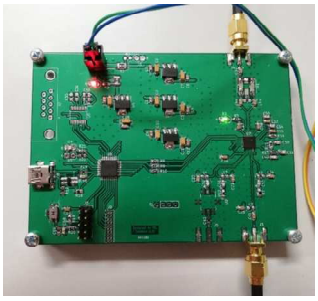
set by writing the control words to its internal registers via a 3-wire serial bus. And the bandwidth of the PLL can be set by an external passive loop filter. Besides of communicating with the PLL, the MCU also provides UART and USB ports for data transmission with computers.



(a). Functional block diagram of integral/fractional PLL module



(b). Prototype of integral/fractional PLL module

Fig. 2: Integral/Fractional PLL module

C. *Control and logic module*

The control & logic module is used to implement integrated low-jittering digital circuits and perform data transmission. As described in Figure 3, the control & logic module consists of two main parts: a MCU which is used as the control and communication unit, and a CPLD which contains large scale integrated logic cells where a wide range of time and frequency components can be implemented by internal low-jittering logic and timing circuits.

Since low jittering is crucial to the time and frequency application, Altera MAX V series chip CPLD MAX5M1270Z is selected as the logic cells. The benefit of CPLD compared to FPGA is its low jittering effect due to its internal macro-cells structure. By downloading the hardware description language (HDL) such as VHDL to the CPLD chip, integrated logic and timing circuits can be implemented such as frequency dividers, counters, phase shifters, digital filters, and etc.

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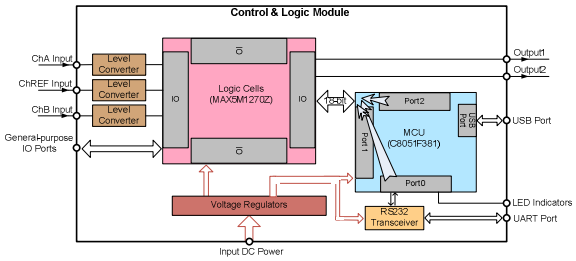

(a). Functional block diagram of control&logic module

(b). Prototype of control&logic module

Fig. 3: Control&Logic module

D. *Power regulator module*

A power regulator module is the auxiliary module which provides low-noise and stable DC power to multiple modules. The power supply module consists of parallel precise voltage regulators to clean-up the noise from the input power supply and satisfy diverse voltage source demands.

III. APPLICATIONS OF UNIVERSAL MODULES

Based on the universal modules, a variety of devices and TF system can be developed. In particular, three applications are demonstrated in this section: an 8-channel frequency distributor, a phase/frequency offset generator, a frequency stability test-set, and a phase comparator.

A. *8-channel frequency distributor*

An 8-channel frequency distributor can be built based on multiple input/output buffers as shown in Figure 4. An input buffer is set in the front stage for impedance matching as well as signal isolation. An integrated power splitter is connected to the output of the front-stage buffer for signal power distribution. 8-channel of output buffers are connected to each output port of the power splitter, respectively, which match the impedance of the load signal in addition to the amplification of the distributed input signal. By sufficient isolation in both input and output stages, total channel isolation can be guaranteed in this structure.

B. *Phase/frequency offset generator*

A high-resolution phase/frequency offset generator can be assembled by universal modules as shown in Figure 5, where

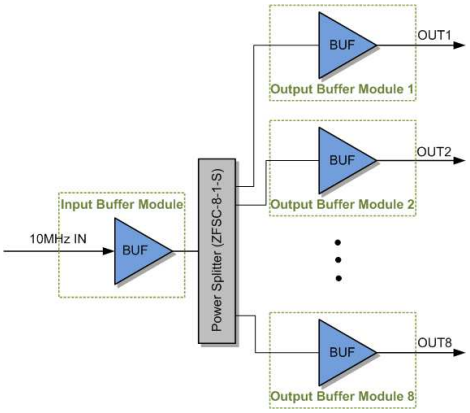

Fig. 4: Block diagram of an 8-channel frequency distributor

the phase and frequency of the output signal (e.g. 1PPS) is adjustable with respect to the input reference signal (e.g. 10MHz or 5MHz). The working principle of the phase/frequency offset generator can be concluded as follows: as shown in Figure 5, after an input buffer module, the reference signal is sent to the fractional PLL module where a frequency or fractional phase offset is generated according to the commands from PC. At the later stage, the control&logic module is programed with a phase shifter which shifts the integral number of phase cycles to the reference signal and an integral frequency divider which down-converts the reference signal to a desired output frequency. Both the nominal frequency of the input and output signals can be programed according to users' needs.

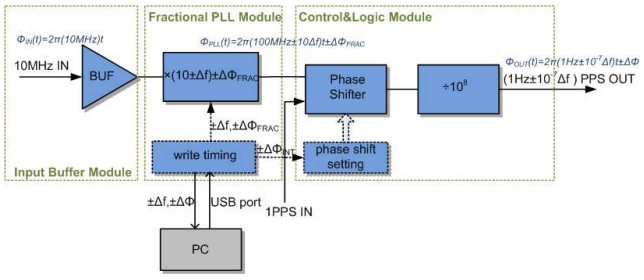

Fig. 5: Block diagram of a phase/frequency offset generator

C. *Frequency stability test-set*

The structure of a heterodyne-based frequency stability test-set is described in Figure 6, following the working principle that phase information is preserved in a mixing process. The test-set generates a frequency offset between two input sources and then measures the beat-frequency continuously to record the average frequency within the specific time interval. In one of the input channels, an integral PLL module is served as an integral frequency multiplier in order to amplify the noise in the input signal. In the other input channel, a fractional PLL module is used as a fractional multiplier to generate a beat-frequency in addition to the integral multiplier. Inside of the control&logic module, a digital mixer, a series of filters, and a counter are cascaded in its internal logic cells for beat-frequency measurements. And the output data can be transmitted through the communication port of the control module to a PC.

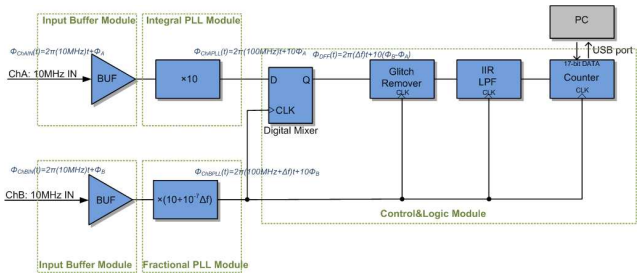

Fig. 6: Block diagram of a frequency stability test-set

IV. FIRST TEST RESULTS

Figure 7 shows the frequency stability test results of a "universal module" based frequency stability test-set. The structure of the test-set is indicated in Figure 6.

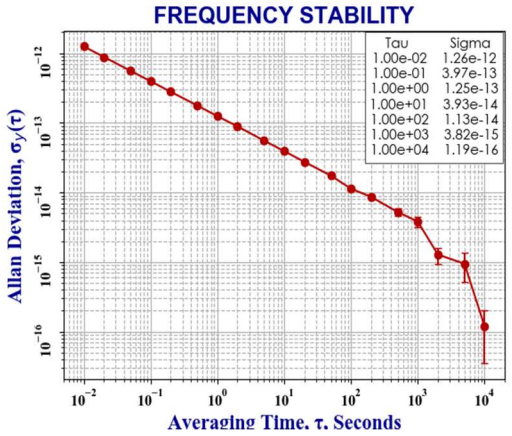

Fig. 7: First frequency stability test results of a "universal module" based frequency stability test-set

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